Claims

1. A heat dissipating silicon-on-insulator (SOI) structure having a buried oxide layer interposed between a silicon layer, including circuitry, and silicon substrate wherein an electrical source is connected to the silicon substrate, whereby the charge carrier flow travels in a direction from the hot region on the SOI structure outward toward the perimeter of the silicon substrate.

2. The structure in claim 1 wherein at least a portion of the silicon substrate is doped to yield an N-type region.

3. The structure in claim 1 wherein an electric via connects the silicon layer with the silicon substrate in order to provide electrical power.

4. The structure in claim 1 wherein the silicon substrate is electrically in series with an electrical load other than itself.

5. The structure in claim 1 wherein the silicon substrate is utilized as a resistive load for an electronic component.

6. A heat dissipating silicon-on-insulator structure having a buried oxide layer interposed between a silicon layer and silicon substrate, the structure comprising:

at least one electrically conductive member attachable to the silicon substrate; and

an electrical source connected to the electrically conductive member, whereby the charge carrier flow travels in a direction from the hotter region on the SOI structure outward toward the perimeter of the silicon substrate.

7. The structure in claim 6 wherein an electric via connects the silicon layer with the silicon substrate in order to provide electrical power to the electrically conductive member.

8. The structure in claim 6 wherein the electrically conductive member is electrically in series with an electrical load other than itself.

9. The structure in claim 6 wherein the electrically conductive member is utilized as a resistive load for an electronic component.

10. The structure in claim 6, further comprising a package for housing the silicon substrate.

11. The structure in claim 6 wherein the SOI structure is attached to the electrically conductive member by wafer bonding.

12. The structure in claim 6 wherein the SOI structure attachment to the electrically conductive member is electrically conductive.

13. A heat dissipating silicon-on-insulator structure having a buried oxide layer interposed between a silicon layer and silicon substrate, said substrate comprising:

at least one thermoelement couple, said couple comprised of the silicon substrate and at least one dissimilar conductor electrically bonded to the silicon substrate thereby creating junctions; and

said thermoelement couple comprises at least one heat absorbing junction and at least one heat rejecting junction wherein the heat absorbing junction is positioned near the center of the SOI substrate and the heat rejecting junction is positioned near the perimeter of the substrate.

14. The structure in claim 13 wherein at least a portion of the silicon substrate is doped to yield an N-type region.

15. The structure in claim 13 wherein the dissimilar conductor comprises more than one layer.

16. The structure in claim 13 wherein an electric via connects the silicon layer with the silicon substrate in order to provide electrical power to the thermoelement couple junctions.

17. The structure in claim 13 wherein a voltage is applied to the thermoelement couple.

18. The structure in claim 13 wherein the thermoelement couple is electrically in series with an electrical load other than itself.

19. The structure in claim 13 wherein the thermoelement couple is utilized as a resistor for an electronic component.

20. The structure in claim 13 wherein a voltage and current is generated by the thermoelement couple and is consumed by an external electric load.

21. The structure in claim 13 wherein the silicon substrate and dissimilar thermoelement, comprising each thermoelement couple, is electrically bonded to each other at both the heat absorbing and heat rejecting junctions thereby creating closed electrical circuit thermoelement couples.

22. A heat dissipating silicon-on-insulator structure, the structure comprising an SOI structure consisting of a buried oxide layer interposed between a silicon layer and silicon substrate, the silicon substrate attachable to a heat sink/spreader structure comprising:

a heat sink/spreader structure wherein at least one thermoelement couple is created through the bonding between at least one semiconductor to at least one dissimilar conductor; and

the dissimilar conductor comprises at least one heat absorbing junction and at least one heat rejecting junction.

23. The structure in claim 22 wherein the heat absorbing junction is positioned near the center of the SOI substrate and the heat rejecting junction is positioned near the perimeter of the substrate.

24. The structure in claim 22 wherein the dissimilar conductor and semiconductor each comprise more than one layer.

25. The structure in claim 22, further comprising a package for housing the silicon substrate.

26. The structure in claim 22 wherein the SOI structure is attached to the heat sink/spreader structure by wafer bonding.

27. The structure in claim 22 wherein the heat sink/spreader structure face to be wafer bonded is larger in overall area than the SOI structure.

28. The structure in claim 22 wherein the heat rejecting junctions are located outside the bond line between the SOI substrate and heat sink/spreader structure.

29. The structure in claim 22 wherein the SOI structure attachment to the heat sink/spreader structure is electrically conductive.

30. The structure in claim 22 wherein a voltage is applied to the thermoelement couple.

31. The structure in claim 22 wherein the thermoelement couple is electrically in series with an electrical load other than itself.

32. The structure in claim 22 wherein the thermoelement couple is utilized as a resistive load for an electronic component.

33. The structure in claim 22 wherein a voltage and current is generated by the thermoelement couple and is consumed by an external electric load.

34. A method of manufacturing a heat dissipating silicon-on-insulator structure, the structure comprising an SOI structure consisting of a buried oxide layer interposed between a silicon layer and silicon substrate, more than one thermoelement couple, each with at least one heat absorbing and one heat rejecting junction and P-type and negative-type N-type conductivity dopants comprising:

(a) Selectively depositing the P and N-type dopants into at least one face of the substrate to form a pattern of P and N-type conductivity thermoelements within the silicon substrate;

(b) Electrically bonding the P and N-type conductivity thermoelements at heat absorbing and heat rejecting junctions to form thermoelement couples.

35. The method of claim 34 wherein the heat absorbing junctions are positioned near the center of the SOI substrate and the heat rejecting junctions are positioned near the perimeter of the substrate.

36. The method of claim 34 wherein a dielectric, such as oxide or nitride, is added to the physical regions between each P and N-type thermoelement in order to provide electrical insulation between each thermoelement.

37. The method of claim 34 wherein the physical regions between each P and N-type thermoelement are removed in order to provide electrical insulation between each thermoelement.

38. The method of claim 34 wherein a voltage is applied to at least one thermoelement couple.

39. The method of claim 34 wherein the thermoelement couple is electrically in series with an electrical load other than itself.

40. The method of claim 34 wherein the thermoelement couple is utilized as a resistive load for an electronic component.

41. The method of claim 34 wherein a voltage and current is generated by at least one thermoelement couple and is consumed by an external electric load.

42. A heat dissipating silicon-on-insulator structure, the structure comprising an SOI structure consisting of a buried oxide layer interposed between a silicon layer and silicon substrate, more than one thermoelement couple stage, each stage containing at least one thermoelement couple, each with at least one heat absorbing and heat rejecting junction, wherein all thermoelement couple stages are fabricated within at least one silicon substrate.

43. The structure in claim 42 wherein each successive thermoelement couple stage is laterally displaced from the previous stage and the heat source.

44. The structure in claim 42 wherein each stage is positioned outside the entire perimeter of the previous stage and each successive stage.

45. The structure in claim 42 wherein each heat absorbing junction is positioned near the center of each thermoelement couple stage and heat rejecting junction is positioned near the perimeter of each stage.

46. The structure in claim 42 wherein a dielectric, such as oxide or nitride, is added to the physical regions between each thermoelement stage in order to provide electrical insulation between each thermoelement.

47. The structure in claim 42 wherein a voltage is applied to at least one thermoelement couple.

48. The structure in claim 42 wherein the thermoelement couple is electrically in series with an electrical load other than itself

49. The structure in claim 42 wherein the thermoelement couple is utilized as a resistive load for an electronic component.

50. The structure in claim 42 wherein a voltage and current is generated by at least one thermoelement couple and is consumed by an external electric load.

51. The structure in claim 42 wherein each dissimilar thermoelement, comprising each thermoelement couple, is electrically bonded to each other at both the heat absorbing and heat rejecting junctions thereby creating closed electrical circuit thermoelement couples.

52. A method of manufacturing a heat dissipating silicon-on-insulator wafer, the wafer includes a top silicon wafer and bottom silicon wafer wherein the bottom wafer comprises at least one thermoelement couple, the couple includes at least two dissimilar thermoelements with at least one heat absorbing and more one heat rejecting junction comprising the steps of:

(a) Applying an oxide layer between the top silicon wafer and the bottom silicon wafer;

(b) Wafer bonding the top silicon wafer to the bottom silicon wafer via the oxide layer.

53. The method of claim 52 wherein the heat dissipating silicon-on-insulator wafer comprises more than one die.

54. The method of claim 52 wherein the heat absorbing junctions are positioned near the center of at least one bottom silicon wafer die and the heat rejecting junctions are positioned near the perimeter of at least one bottom silicon wafer die.

55. The method of claim 52 wherein the thermoelement couple is formed by selectively depositing the P and N-type dopants into at least one face of the bottom silicon wafer to form a pattern of P and N-type conductivity thermoelements within at least one bottom silicon wafer die.

56. The method of claim 52 wherein the P and N-type conductivity thermoelements are electrically bonded at heat absorbing and heat rejecting junctions to form at least one thermoelement couple within at least one bottom silicon wafer die.

57. The method of claim 52 wherein at least one bottom silicon wafer die contains more than one thermoelement couple stage.

58. The method of claim 52 wherein each successive thermoelement couple stage is laterally displaced from the previous stage and the center of at least one bottom silicon wafer die.

59. The method of claim 52 wherein each stage is positioned outside the entire perimeter of the previous stage and each successive stage.

60. The method of claim 52 wherein a voltage is applied to at least one thermoelement couple.

61. The method of claim 52 wherein the thermoelement couple is electrically in series with an electrical load other than itself.

62. The method of claim 52 wherein the thermoelement couple is utilized as a resistive load for an electronic component.

63. The method of claim 52 wherein a voltage and current is generated by at least one thermoelement couple and is consumed by an external electric load.